Digital Electronics

Name_____ ID_____ TA_____

Partners_____

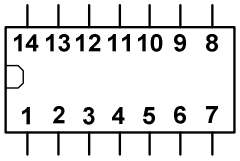
Date_____ Section_____

Please do not remove chips from the breadboard of the electronics trainer, since the pins are delicate and easily damaged. If you need to, please ask the TA.

1. The testing of gates in four types of chips

Pin	74LS00 NAND	✔	74LS02 NOR	✔	74LS04 NOT	✔	74LS08 AND	✔
1	1A		1Y		1A		1A	
2	1B		1A		1Y		1B	
3	1Y		1B		2A		1Y	
4	2A		2Y		2Y		2A	
5	2B		2A		3A		2B	
6	2Y		2B		3Y		2Y	
7	Ground	-	Ground	-	Ground	-	Ground	-
8	3Y		3A		4Y		3Y	
9	3A		3B		4A		3A	
10	3B		3Y		5Y		3B	
11	4Y		4A		5A		4Y	
12	4A		4B		6Y		4A	
13	4B		4Y		6A		4B	
14	VCC	-	VCC	-	VCC	-	VCC	-

Pin numbering of chips



***If you find broken gates in chips, please let the TA know, and replace them with new ones.**

➢ The truth table for above gates

inputs		outputs		
A	B	$Y_{NAND} = \overline{A \cdot B}$	$Y_{NOR} = \overline{A + B}$	$Y_{AND} = A \cdot B$
0	0	1	1	0
0	1	1	0	0
1	0	1	0	0
1	1	0	0	1

inputs	outputs
A	$Y_{NOT} = \overline{A}$
0	1
1	0

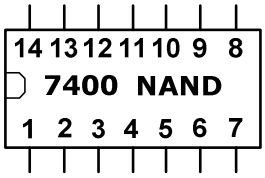
2. XOR implementations

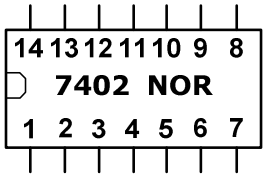
- Algebraic expression $A \oplus B = \left(A \cdot \overline{B}\right) + \left(\overline{A} \cdot B\right)$
- Draw the circuit diagram (You cannot use OR gates.)

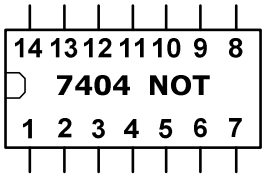
*Truth table for XOR

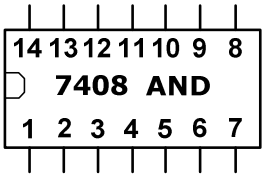
inputs		outputs
A	B	$Y_{XOR}=A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

- Wire connections







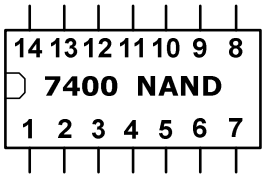


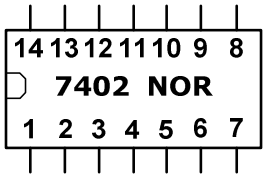
- Algebraic expression $A \oplus B = \overline{\left(\overline{A} \cdot \overline{B}\right)} \cdot \overline{\left(A \cdot B\right)}$
- Draw the circuit diagram (You cannot use OR gates.)

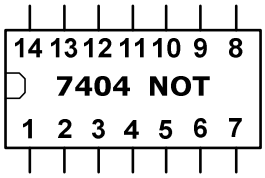
*Truth table for XOR

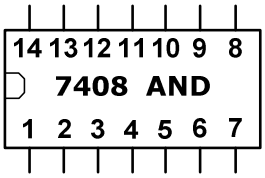
inputs		outputs
A	B	$Y_{XOR}=A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

- Wire connections









3. The test of DeMorgan's theorem

- The verification of $\overline{A} \cdot \overline{B} = \overline{A + B}$. (The TA will show how to do this part. So please copy what he/she did in the spaces provided.)

$\overline{A} \cdot \overline{B}$ *Truth Table

*circuit diagram		A	B	$Y = \overline{A} \cdot \overline{B}$

$\overline{A + B}$ *Truth Table

*circuit diagram		A	B	$Y = \overline{A + B}$

- The verification of $\overline{A} + \overline{B} = \overline{A \cdot B}$. (You will draw the circuit diagrams and truth tables. In addition, you are going to **see if the truth table is correct with the actual connections on the "Circuit Trainer."**)

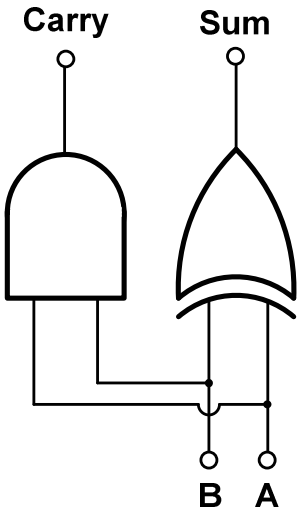
$\overline{A} + \overline{B}$ *Truth Table

*circuit diagram		A	B	$Y = \overline{A} + \overline{B}$

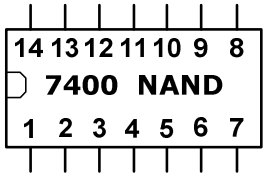
$\overline{A \cdot B}$ *Truth Table

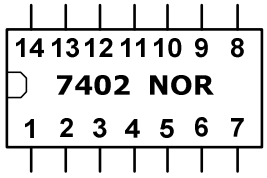
*circuit diagram		A	B	$Y = \overline{A \cdot B}$

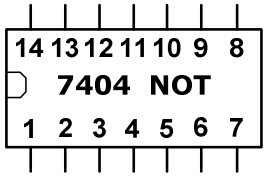
4. Implementation of a half adder circuit

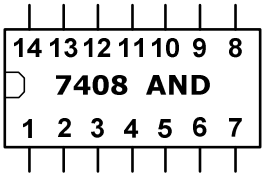


- Draw the wire connections for the half adder.









Please show (perform) your results to the TA before you leave. Thanks!

Lab Procedure for Digital Electronics

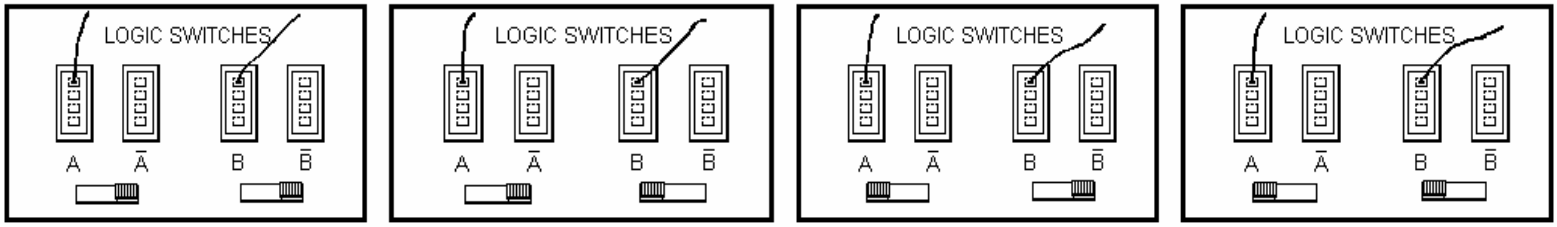
Please notice we do not have OR gates to construct a circuit. You have to make use of NOR gates for that.

1. The testing of gates in four types of chips

- **Connect 4 kinds of chips on the breadboard in series.**
  You do not have to take those from the board even after the lab.

- **Connect pin #7 to Ground with one wire, and pin #14 to 5V with another wire.**
  Otherwise, you will not get right results.

- **Using 3 more wires, test all 18 gates.**
  Procedure:
  1. See the pin connection table on the data sheet. 'A' and 'B' denote the inputs, and 'Y' denotes the output of a gate.
  2. The wire for an <u>output</u> will be connected to "logic probe" on the Circuit Trainer.
  3. With referring to the truth table on the data sheet, you will combine the two inputs 'A' and 'B.' See the figures given below.



  4. From left, 0-0 input, 0-1 input, 1-0 input, and 1-1 input. In fact, '0' corresponds to 0-volt, and '1' corresponds to 5-volt inputs.

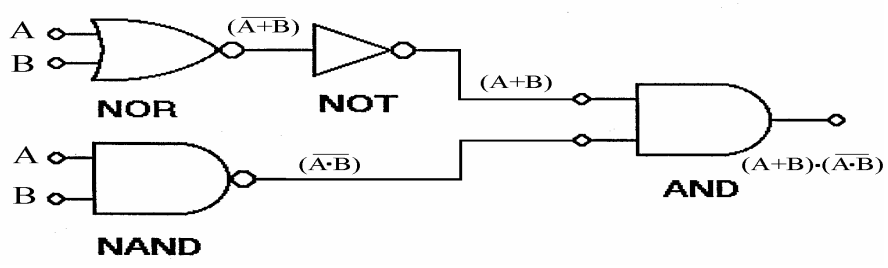
- **Check each box for a gate when it is working properly.**
  If one of gate was totally damaged, please tell TA about that. He/She will give you another one. However, if only one or two gates are broken in a chip, just check those and try not using them for the second part.

2. XOR implementations

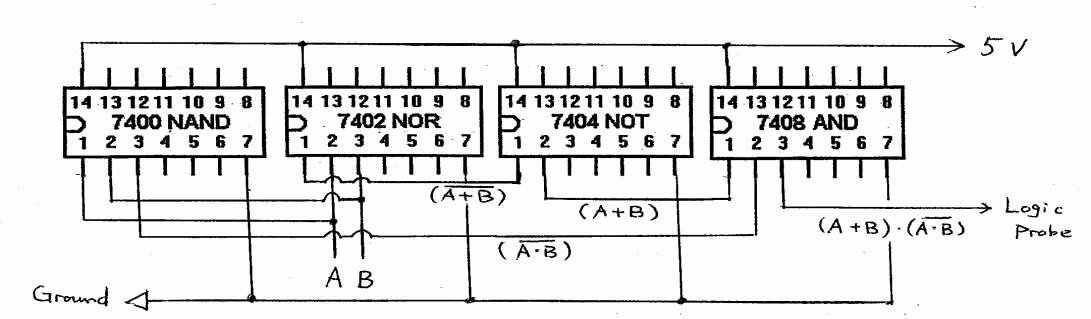
- **You will test 3 different digital circuits to accomplish XOR outputs. The first one will be the following:** (The TA will show how to do these, and then you will do the same thing for the rest of those.) *Note: *For NOR gates, the pattern of inputs and out put is different from AND and NAND gates.*

  ◆Algebraic Expression $A \oplus B = (A + B) \cdot \left(\overline{A \cdot B}\right)$

  ◆Circuit Diagram



◆Actual Circuit Connections



- **The TA will show the circuit diagram for the second one, as well. Then you will be able to do the rest.**
  Once you understand how to do this part, the rest is straightforward.

- **Do not forget to see if the outputs are the same as the truth table shown on the data sheet.**

Please turn off the power of the Circuit Trainer when you connect the wires to the chips. Otherwise, the chips will be burned.

3. The test of DeMorgan's theorem

- **Connect pin #7 to Ground with one wire, and pin #14 to 5V with another wire.**
  Otherwise, you will not get right results.

- **As the TA explained for $\overline{A} \cdot \overline{B} = \overline{A + B}$, prove the equation, $\overline{A} + \overline{B} = \overline{A \cdot B}$.**

  Procedure:
  1. Draw the circuit diagram on the data sheet.
  2. Guess the truth table by using the truth tables of the other gates.
  3. If you like, you can draw the wire connections on a scratch paper. Then connect the wires on the breadboard to make sure if the equation is correct. (It must be correct!)

4. Implementation of a half adder circuit

- **Make sure if pins #7 and pins #14 are connected to Ground and to 5V respectively.**

- **First, implement an XOR output.**
  It is recommended you use this, $A \oplus B = (A + B) \cdot \left(\overline{A \cdot B}\right)$ to implement XOR. Refer to part two of this lab.

- **Make sure if the XOR outputs are correct.**
  Please see the reference paper that the TA provided for each table.

- **With referring to the circuit diagram on data sheet, implement the half adder circuit.**

Inputs, A and B will go to the LOGIC SWITCHES section on the Circuit Trainer so that you can change the combinations easily. (If those do not work, please use the Binary Data.) According to the circuit, you must have 2 outputs. From the XOR gate, it will go to 'L0', and from the AND gate, it will go to L1 in the Logic Indicators so that it can be displayed easily.

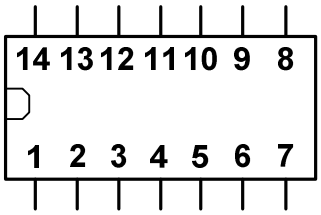
5. Lab report

- **Please state what you learned from this lab.**
  This lab does not generate uncertainties or errors, so you will not discuss those. Of course, you can state what you did not understand on this lab.

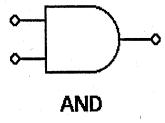
Reference for Digital Electronics Lab

- **Pin connections of logic gates**

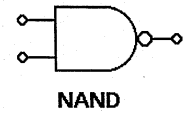
pin #	74LS00 NAND	74LS02 NOR	74LS04 NOT	74LS08 AND
1	1A	1Y	1A	1A
2	1B	1A	1Y	1B
3	1Y	1B	2A	1Y
4	2A	2Y	2Y	2A
5	2B	2A	3A	2B
6	2Y	2B	3Y	2Y
7	Ground	Ground	Ground	Ground
8	3Y	3A	4Y	3Y
9	3A	3B	4A	3A
10	3B	3Y	5Y	3B
11	4Y	4A	5A	4Y
12	4A	4B	6Y	4A
13	4B	4Y	6A	4B
14	Vcc	Vcc	Vcc	Vcc



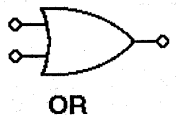
- **Truth tables**



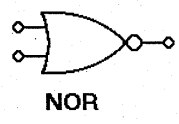
A	B	Y_{AND}
0	0	0
0	1	0
1	0	0
1	1	1



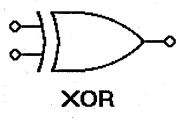
A	B	Y_{NAND}
0	0	1
0	1	1
1	0	1
1	1	0



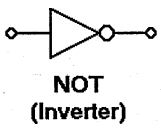
A	B	Y_{OR}
0	0	0
0	1	1
1	0	1
1	1	1



A	B	Y_{NOR}
0	0	1
0	1	0
1	0	0
1	1	0



A	B	Y_{XOR}
0	0	0
0	1	1
1	0	1
1	1	0



A	Y_{NOT}
0	1
1	0