

# Digital Electronics I

Name \_\_\_\_\_ ID \_\_\_\_\_ TA \_\_\_\_\_

Partners \_\_\_\_\_

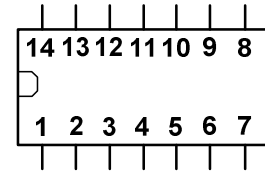
Date \_\_\_\_\_ Section \_\_\_\_\_

**Please do not remove chips from the breadboard of the electronics trainer, since the pins are delicate and easily damaged. If you need to, please ask the TA.**

## 1. The testing of gates in four types of chips

Pin	74LS00 NAND	✓	74LS02 NOR	✓	74LS04 NOT	✓	74LS08 AND	✓
1	1A		1Y		1A		1A	
2	1B		1A		1Y		1B	
3	1Y		1B		2A		1Y	
4	2A		2Y		2Y		2A	
5	2B		2A		3A		2B	
6	2Y		2B		3Y		2Y	
7	Ground	-	Ground	-	Ground	-	Ground	-
8	3Y		3A		4Y		3Y	
9	3A		3B		4A		3A	
10	3B		3Y		5Y		3B	
11	4Y		4A		5A		4Y	
12	4A		4B		6Y		4A	
13	4B		4Y		6A		4B	
14	VCC	-	VCC	-	VCC	-	VCC	-

Pin numbering of chips



**\*If you find broken gates in chips, please let the TA know, and replace them with new ones.**

➤ The truth table for above gates

inputs		outputs		
A	B	$Y_{NAND} = \overline{A \cdot B}$	$Y_{NOR} = \overline{A + B}$	$Y_{AND} = A \cdot B$
0	0	1	1	0
0	1	1	0	0
1	0	1	0	0
1	1	0	0	1

inputs	outputs
A	$Y_{NOT} = \overline{A}$
0	1
1	0

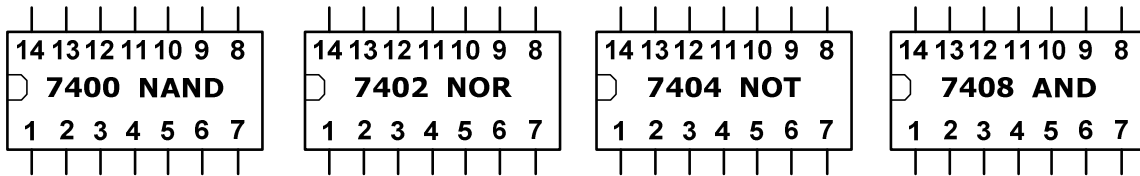
## 2. XOR implementations

- Algebraic expression  $A \oplus B = (A \cdot \bar{B}) + (\bar{A} \cdot B)$
- Draw the circuit diagram (You cannot use OR gates.)

\*Truth table for XOR

inputs		outputs
A	B	$Y_{XOR}=A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

- Wire connections

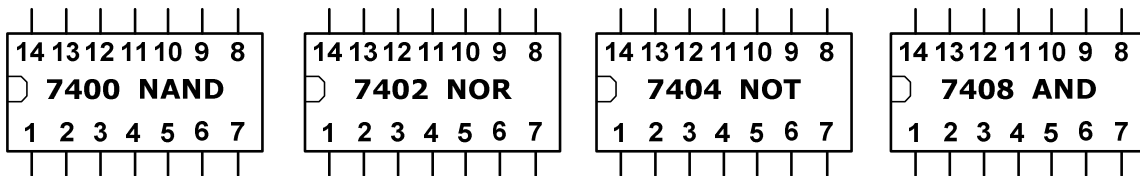


- Algebraic expression  $A \oplus B = \overline{(A \cdot B)} \cdot \overline{(A \cdot B)}$
- Draw the circuit diagram (You cannot use OR gates.)

\*Truth table for XOR

inputs		outputs
A	B	$Y_{XOR}=A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

- Wire connections



## Lab Procedure for Digital Electronics I

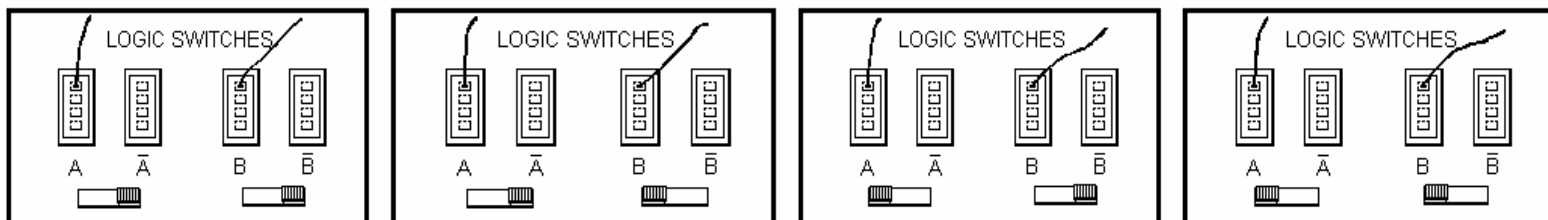
**Please notice we do not have OR gates to construct a circuit. You have to make use of NOR gates for that.**

### 1. The testing of gates in four types of chips

- **Connect 4 kinds of chips on the breadboard in series.**  
You do not have to take those from the board even after the lab.
- **Connect pin #7 to Ground with one wire, and pin #14 to 5V with another wire.**  
Otherwise, you will not get right results.
- **Using 3 more wires, test all 18 gates.**

Procedure:

1. See the pin connection table on the data sheet. 'A' and 'B' denote the inputs, and 'Y' denotes the output of a gate.
2. The wire for an output will be connected to "logic probe" on the Circuit Trainer.
3. With referring to the truth table on the data sheet, you will combine the two inputs 'A' and 'B.' See the figures given below.



4. From left, 0-0 input, 0-1 input, 1-0 input, and 1-1 input. In fact, '0' corresponds to 0-volt, and '1' corresponds to 5-volt inputs.

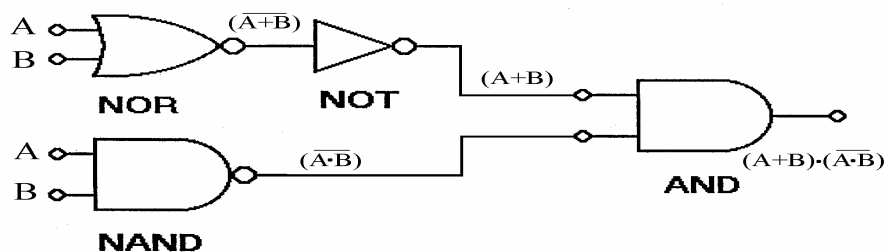
- **Check each box for a gate when it is working properly.**  
If one of gate was totally damaged, please tell TA about that. He/She will give you another one. However, if only one or two gates are broken in a chip, just check those and try not using them for the second part.

### 2. XOR implementations

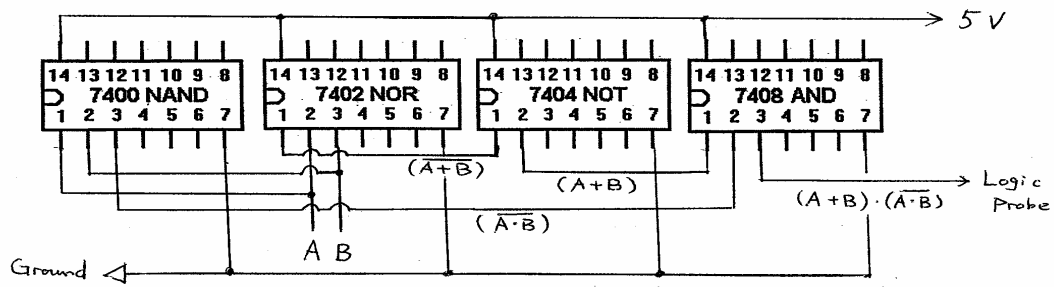
- **You will test 3 different digital circuits to accomplish XOR outputs. The first one will be the following:** (The TA will show how to do these, and then you will do the same thing for the rest of those.) *\*Note: For NOR gates, the pattern of inputs and out put is different from AND and NAND gates.*

◆ Algebraic Expression 
$$A \oplus B = (A + B) \cdot (\overline{A \cdot B})$$

◆ Circuit Diagram



◆ Actual Circuit Connections



- The TA will show the circuit diagram for the second one, as well. Then you will be able to do the rest.  
Once you understand how to do this part, the rest is straightforward.
- Do not forget to see if the outputs are the same as the truth table shown on the data sheet.

### 3. Lab report

- Please state what you learned from this lab.  
This lab does not generate uncertainties or errors, so you will not discuss those. Of course, you can state what you did not understand on this lab.